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| 10/002,085 | 11/01/2001 | William John Goetzinger | ROC920010202US1 | 2023 |

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| EXAMINER | |
|---|---|
| AHMED, SALMAN | |

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| 2616 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/002,085 | GOETZINGER ET AL. | |
| | Examiner | Art Unit | |
| | Salman Ahmed | 2666 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *3/6/06(Amendment)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-24* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/1/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-24 are pending

Claims 1-9, 11-24 are rejected

Claim 10 is objected.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 5, 8, 13, 16, 22 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Meier et al. (U.S. 6,481,251).

The Meier et al. reference teaches all of the limitations of the listed claim with reasoning that follows. Regarding claims 5 and 13 "examining an empty indicator associated with the scheduling queue;" Meier et al. anticipates empty indication for store queue as spoken of column 13, lines 66-67 and column 14, lines 1-4; "refraining from searching the scheduling queue if the empty indicator indicates that the scheduling queue is empty; searching the scheduling queue if the empty indicator indicates that the scheduling queue is not empty; detaching from the scheduling queue a winning flow found in the searching step." Meier et al. anticipates store queue control circuit 74 generates a

mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10.

Regarding claim 24, Meier et al. discloses all the limitations of claim 24 as discussed with claim 13. It should be noted that claim 24 is simply the computer program containing the methods of claim 13.

Regarding claim 22, Meier et al. discloses all the limitations of claim 22 as discussed with claim 5. It should be noted that claim 22 is simply the computer program containing the methods of claim 5.

3. Claims 9, 11, 12 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Naven et al. (U.S. 6,810,043), hereinafter referred to as Naven

The Naven reference teaches all of the limitations of the listed claim with reasoning that follows. Regarding claim 9, "attaching a flow to the scheduling queue" Naven teaches each storage location 2 is capable of storing one or more entries, each such entry denoting that a specified virtual channel is to be serviced by the traffic manager in the

time slot which the storage location corresponds as stated in column 1, lines 58-61. "Placing an empty indicator associated with the scheduling queue in a condition to indicate that the scheduling queue is not empty." Naven discloses the master snoop memory 20 is N bits wide such that each N-bit word 22 corresponds individually to one of the storage locations 2 of the group. In this case, when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein.

Regarding claim 11, "setting a bit in a register" Naven anticipates when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein (column 8, lines 24-26).

Regarding claim 12, "resetting a bit in a register" Naven anticipates if the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty", i.e. does not contain a valid entry (column 8, lines 26-28).

Regarding claim 23, Naven et al. anticipates all the limitations of claim 23 as discussed with claim 9. It should be noted that claim 23 is simply the computer program containing the methods of claim 9.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-4,19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figure 1,2 and 3 in view of Meier et al. (U.S. 6,481,251).

Regarding claim 1, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more schedules queues, each adapted to define a respective sequence in which flows are to be serviced" Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42. Prior Art fails to explicitly teach done or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty." However, Meier et al. in the same field of endeavor teaches empty indication in the empty indicator of Meier et al. in schedule queue of Prior Art in order to indicate weather the respective scheduling queue is empty as spoken of on column 14, lines 2-4 of Meier et al. reference. A motivation for doing so would be, if the scheduling queue

that is searched during a given cycle turns out to be empty, then the cycle may be wasted. Regarding claim 2, Meier et al. further discloses empty indication may be a bit indicating empty when set and indicating not empty when clear, as stated in column 14, lines 5-6.

Regarding claim 3, Applicant's admitted Prior Art further discloses one or more schedule queues 42 include plurality of scheduling queues as shown in Figure 2. Prior Art fails to disclose empty indicators include a plurality of empty indicators. However, Meier et al. in the same field of endeavor in Figure 5, illustrates store queue assignment circuit 60 in response to completion of one or more stores. Additionally, store queue number assignment circuit 60 determines if the head store queues number equals the tail store queue number. If so, the empty indication in empty register 65 is set to indicate empty as stated in column 14, lines 24-48. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to use plurality of empty indicators of Meier et al. along with plurality of scheduling queues of Admitted Prior Art Figure 2. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, then the cycle may be wasted.

Regarding claim 4, Applicant's admitted Prior Art further discloses each scheduling queue 42 includes 512 slots 48 to which flows are attachable as shown in Figure 2 and 3.

Regarding claim 19, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues, each

adapted to define a respective sequence in which flows are to be serviced" Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42. Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty." However, Meier et al. in the same field of endeavor teaches empty indication in the empty register indicates that the store queue is empty. Column 14, lines 2-3 Prior Art fails to teach "examining an empty indicator associated with the first scheduling queue" Meier et al. teaches empty indication for store queue as spoken of column 13, lines 66-67 and column 14, lines 1-4 "refraining from searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is empty; searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is not empty; and detach from the first scheduling queue a winning flow found in the search of the first scheduling queue." However Meier et al. in the same field of endeavor teaches store queue control circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated bf the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, storage queue control circuit! 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10. At the time of the invention, it

would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier et al. in schedule queue of prior Art in order to indicate weather the respective scheduling queue is empty as spoken of on column 14, line 2-4 of Meier et al. reference. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, than the cycle may be wasted.

Regarding claim 21, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues each adapted to define a respective sequence in which flows are to be serviced" Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42. Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty "However, Meier et al. in the same field of endeavor teaches empty indication in the empty register indicates that the store queue is empty. Column 14, lines 2-3. Prior Art fails to teach "examine an empty indicator associated with a first scheduling queue; refrain from searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is empty; search the first scheduling queue if the empty indicator indicates that the first scheduling queue is not empty; if a winning flow is found by the search of the first scheduling queue, detach the winning flow from the first scheduling queue; if no flow is found by the search of the first scheduling queue, place the empty indicator in a condition to indicate that the first scheduling queue is empty." Meier et al. in the same field of endeavor teaches store queue control circuit 74 generates a mask

using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier et al. in schedule queue of Prior Art in to search or not to search if empty indicator indicate empty or not empty as spoken of on column 14, line 2-6 of Meier et al. reference. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, than the cycle may be wasted.

7. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier in view of Naven.

In regards to claims 17 and 18 teaches queue scheduling method as described in the rejections of claim 13 above.

In regards to claims 17, Meier does not explicitly teach detaching step is performed, a further search of the scheduling queue is performed to determine whether

any flows are enqueued in the scheduling queue other than the flow detached in the detaching step. In regards to claims 18, Meier does not explicitly teach empty indicator is placed in a condition to indicate that the scheduling queue is empty if the further search of the scheduling queue determines that there are no flows in the scheduling queue other than the flow detached in the detaching step.

Regarding claim 17, "if the detaching step is performed, a further search of the scheduling queue is performed to determine whether any flows are en-queued in the scheduling queue other than the flow detached in the detaching step." Naven in the same field of endeavor discloses when a bit in the word 22 is set to 1 this denotes that the corresponding storage location 2 has at least one VC entered therein. If the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty" i.e. does not contain a valid entry. Column 8, lines 24-28. Regarding claim 18, "the empty indicator is placed in a condition to indicate that the scheduling queue is empty if the further search of the scheduling queue determines that there are no flows in the scheduling queue other than the flow detached in the detaching step." Naven in the same field of endeavor discloses if the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty", i.e. does not contain a valid entry column 8, lines 26-28.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier's method by incorporating the method of doing further search and setting an indicator as taught by Naven. The motivation is that such additional search will help prevent race condition, i.e. during first search if the state of

the queue changes, it will be detected; thus making the system more robust and less error prone.

8. Claims 6 and14 rejected under 35 U.S.C. 103(a) as being unpatentable over Meier in view of Lyons et al. (Third New Zealand ATM and Broadband Workshop: Title-Estimating Clock Speeds for the ATMSWITCH Architecture).

Regarding claims 6 and 14, Meier et al. teaches empty indicator associated with scheduling queue, refraining from searching the scheduling queue if the empty indicator indicates empty, and searching the scheduling queue if the empty indicator indicates non-empty (see claim 5 and 13). Meier does not teach, selecting the scheduling queue from among a plurality of scheduling queues in a round robin process." Lyons et al. in the same field of endeavor teaches round robin process in ATMSWITCH, At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier et al. and searching the scheduling queue in a round robin server as in Lyons et al. in moves around the circular queue removing a cell from the current cell queue whenever the output port becomes free, and moving on to next queue in time for the next output slot. Column 3, Paragraph 4 lines 6-11 under The ATMSWITCH.

9. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier in view of Lyons in view of Naven.

Regarding claim 7 and 15, Meier teaches empty indicator associated with scheduling queue, refraining from searching the scheduling queue if the empty indicator indicates empty, and searching the scheduling queue if the empty indicator indicates non-empty (see claim a and 13) and Lyons teaches round robin process (see claim 6 and 14). Meier et al. and Lyons et al does not teach "searching step includes a plurality of sub-queues includes in the scheduling queue, the sub-queues having mutually different respective ranges and resolutions." However in further view of Naven et al., Naven in the same field of endeavor teaches that the master calendar (scheduling queue) and slave calendar (sub-queues) are plurality of storage locations corresponding respectively to a succession of time slots (column 4 lines 44-45). It can also be seen from figure 2 that the slave calendar and master calendar have a different number of time slots. It should be obvious to a person skilled in the art given these references to have different ranges and resolutions for sub-queues. A motivation for doing so would be the master calendar and slave calendar have the different range and resolution of slots (the scheduling queue has different number of slots that is different than a number slots of the sub-queue, 7 and 2 of figure 2).

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art Figure 1,2 and 3 in view of Meier in view of Naven.

Regarding claim 20, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues, each adapted to define a respective sequence in which flows are to be serviced" Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42. Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty." However, Meier et al. in the same field of endeavor teaches empty indication in the empty register indicates that the store queue is empty. Column 14, lines 2-3 Prior Art and Meier et al. fails to teach "attach a flow to the first scheduling queue" Naven teaches each storage location 2 is capable of storing one or more entries, each such entry denoting that a specified virtual channel is to be serviced by the traffic manager in the time slot which the storage location corresponds as stated in column 1, lines 58-61; place an empty indicator associated with the first scheduling queue in a condition to indicate that the first scheduling queue is not empty." Naven discloses the master snoop memory 20 is N bits wide such that each N-bit word 22 corresponds individually to one of the storage locations 2 of the group. In this case, when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier et al. in schedule queue of Prior Art in order to indicate weather the respective scheduling queue is not empty as spoken of on column 14, line 2-6 of Meier et al. reference. A

motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, than the cycle may be wasted.

### *Allowable Subject Matter*

11. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

12. Applicant's arguments, page 6-9 of the Remarks section, filed 3/6/2006, with respect to the rejections of claims 5, 8, 13, 16 and 24 have been fully considered but they are not persuasive. Applicant argues the cited passage of Meier appears to be describing a pointer that is reset when the pointer has reached the end of a '"store queue" and an indicator that gets used to indicate not empty when the pointer has reached the end of the store queue. Applicant argues the empty indication described in Meier does not appear to refer to an indicator that reflects whether data flows are present in a scheduling queue. In other words, the Examiner has not identified, and Applicant cannot find, any teaching or even suggestion within Meier that discloses an indicator that reflects whether data flows are present in a scheduling queue. However, examiner respectfully disagrees with this assertion. The present claim language is broad and in view of the broadest reasonable interpretation of this language, Meier does teach the limitations stated above. To further clarify, Meier teaches during execution of

the load, the load's store queue number (in combination with the head store queue number) identifies the store queue entries on which the load may hit. If the store queue is empty (as indicated by an empty indication stored in empty register 65) when a load is received by store queue number assignment circuit 60, store queue number assignment circuit 60 indicates that the store queue number assigned to the load is invalid (and thus the load does not hit any store queue entries) (column 10 lines 20-28).

Applicant further argues detaching from the scheduling queue a winning flow found in the searching step appears to be distinct from the recited feature of the present invention, which involves dequeutng a data flow found in the searching step. However, examiner respectfully disagrees with this assertion. The present claim language is broad and in view of the broadest reasonable interpretation of this language, Meier does teach the limitations stated above.

Applicant's arguments, page 9-10 of the Remarks section, filed 3/6/2006, with respect to the rejections of claim 9 has been fully considered but they are not persuasive. Applicant argues Naven reference does not appear to describe setting an empty/non-empty indicator for data flows in a scheduling queue. However, examiner respectfully disagrees with this assertion. The present claim language is broad and in view of the broadest reasonable interpretation of this language, Naven does teach the limitations stated above.

13. Applicant's arguments, page 10-12 of the Remarks section, filed 3/6/2006, with respect to the rejections of claims I -4, 6, 7, 11, 15, 19 - 22, and 24 have been fully considered but they are not persuasive for the reasons stated above.

14. Applicant's arguments, page 10-12 of the Remarks section, filed 3/6/2006, with respect to the rejections of claims 7, 10- 12, 15, 17, 18, 20 and 23 have been fully considered but they are not persuasive for the reasons stated above.

15. Applicant's arguments, page 10-12 of the Remarks section, filed 3/6/2006, with respect to the rejections of claims 1, 3, 19, 20, and 21 have been fully considered but they are not persuasive. Applicant argues rejections of Claims 1, 3, 19, 20, and 21 are further untenable because the Examiner has not provided a proper motivation to combine the art described in Applicant's Background section with Meier. However, examiner respectfully disagrees with this assertion. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art at the time the invention was made. See In re Keller 642 F.2d 413, 208 USPQ 871 (CCPA 1981.

16. Applicant's arguments, page 12 of the Remarks section, filed 3/6/2006, with respect to the rejections of claims 10 has been fully considered but they are persuasive.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571)272-8307. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571)272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 2666

SA

03/18/2006

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